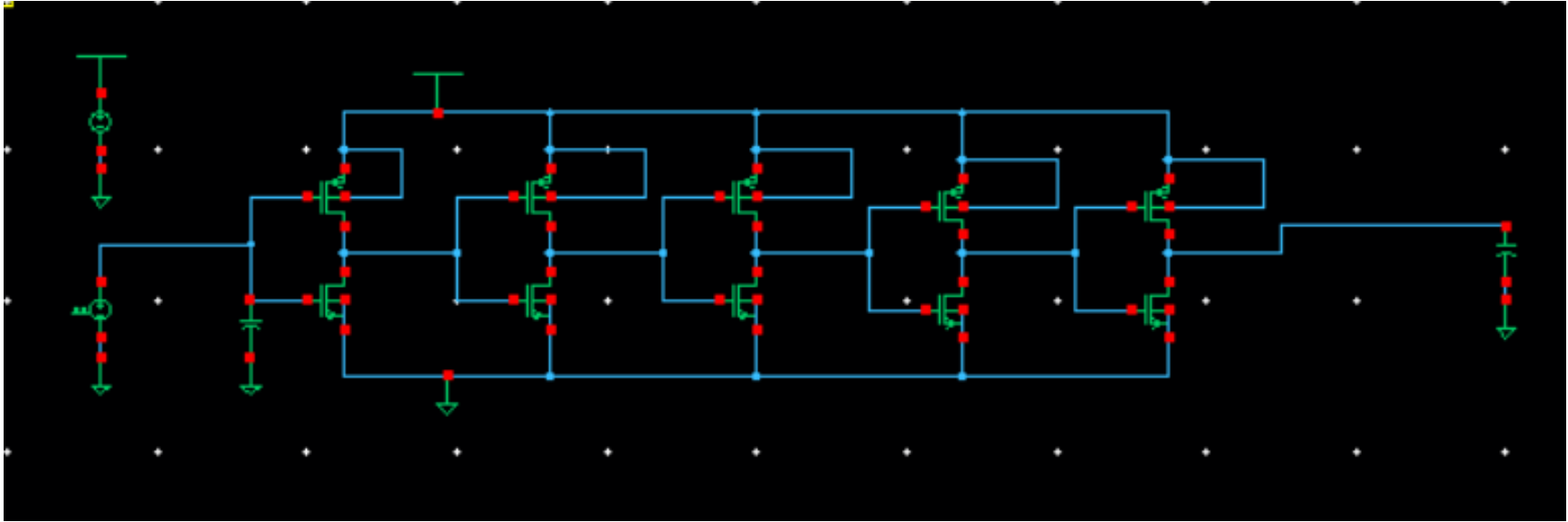


# 467 project

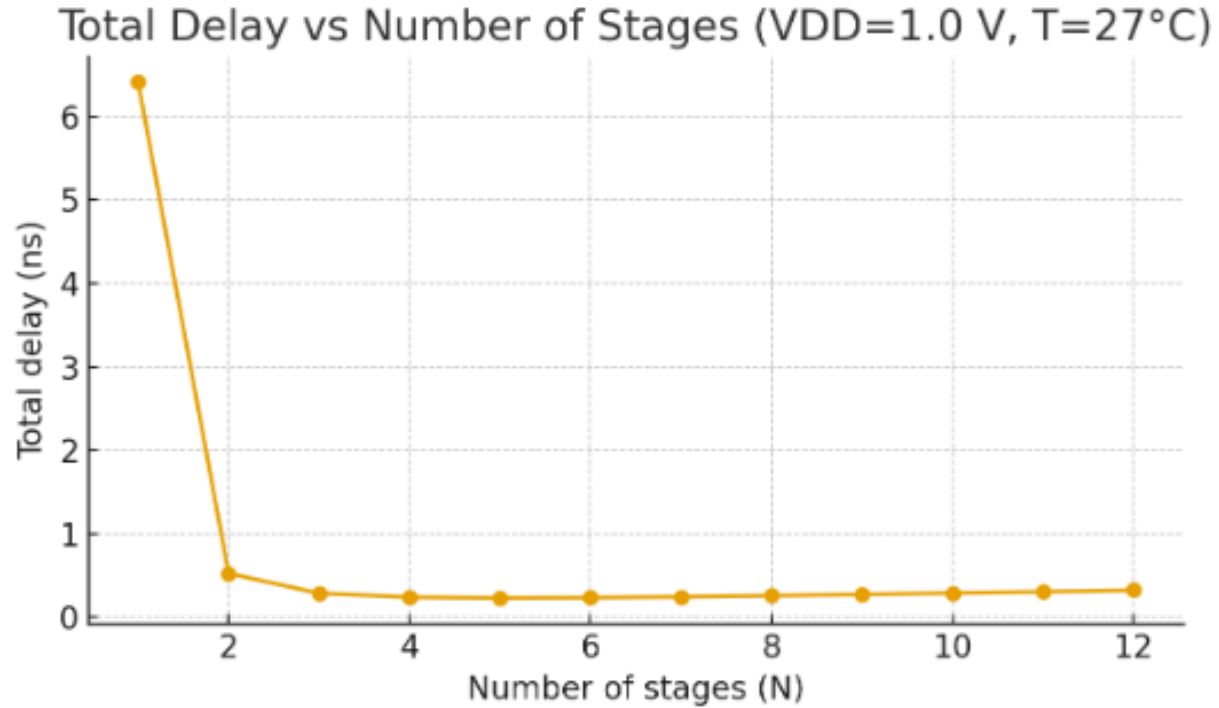
Dalton Reynolds, Tessa Urwin, Julian O'Hern, Lucas Bigos

# Inverter Chain

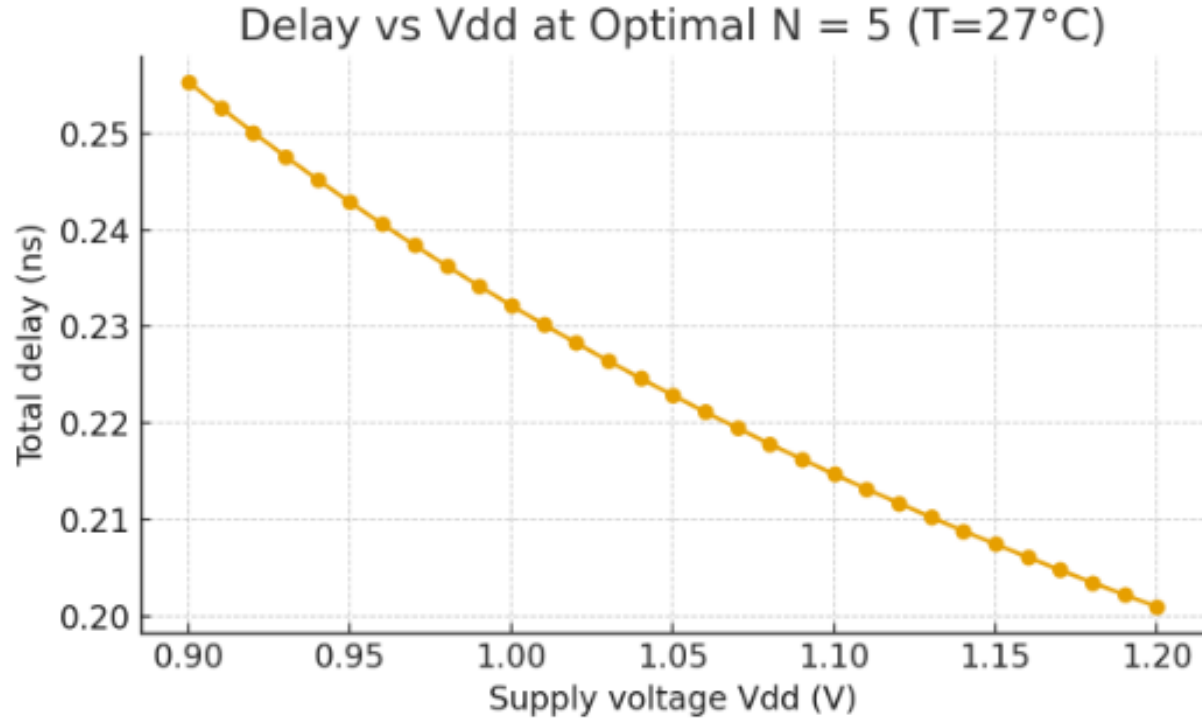
- Schematic :



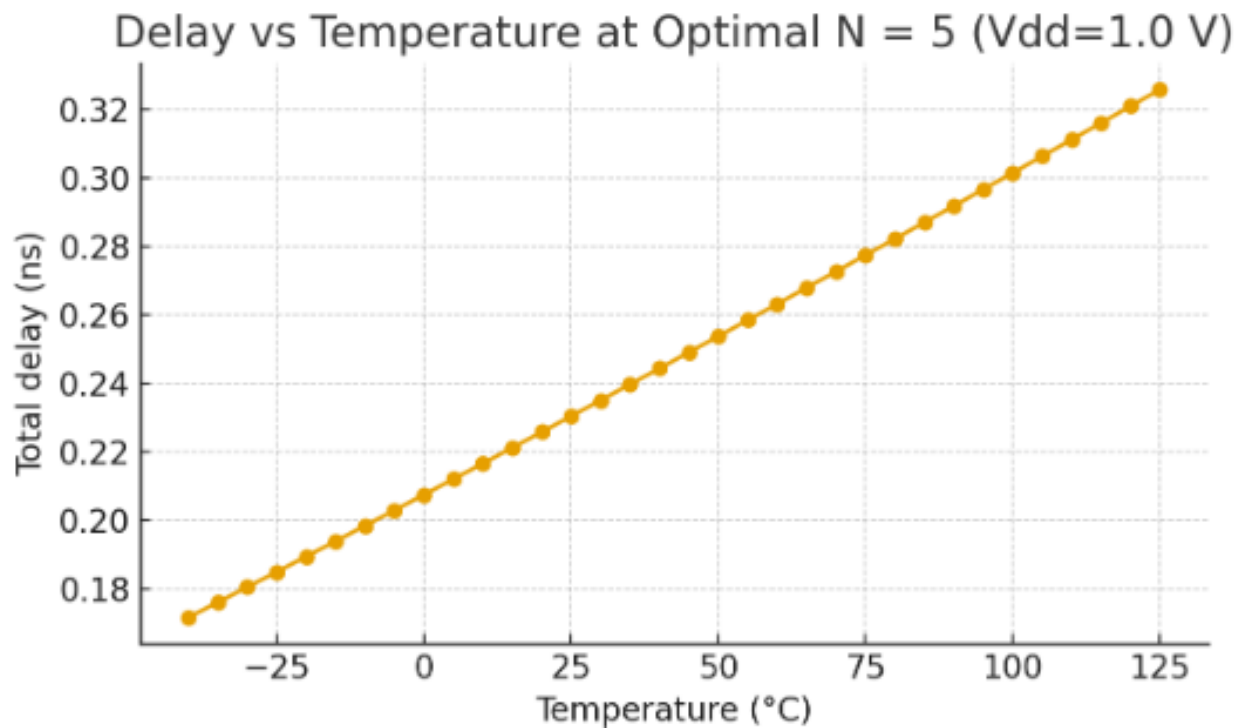
## delay vs. number of stages (N)



## delay vs. supply voltage



## delay vs. temperature

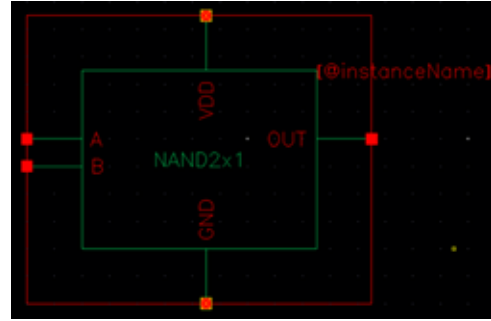
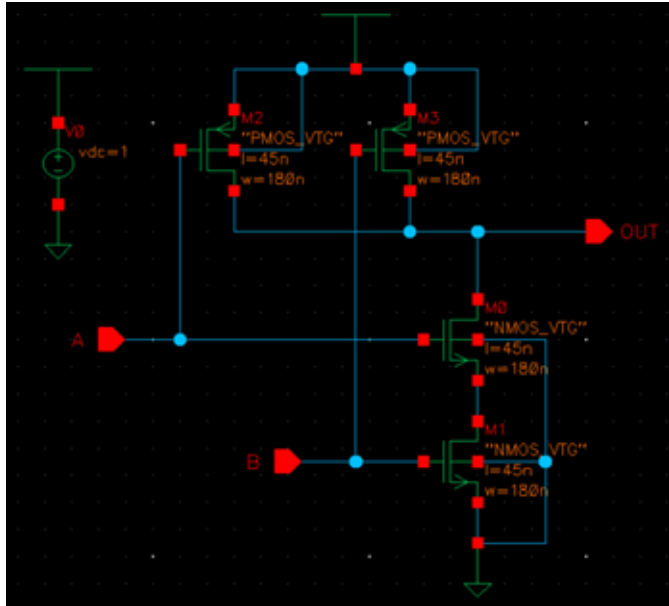


# Cell Library

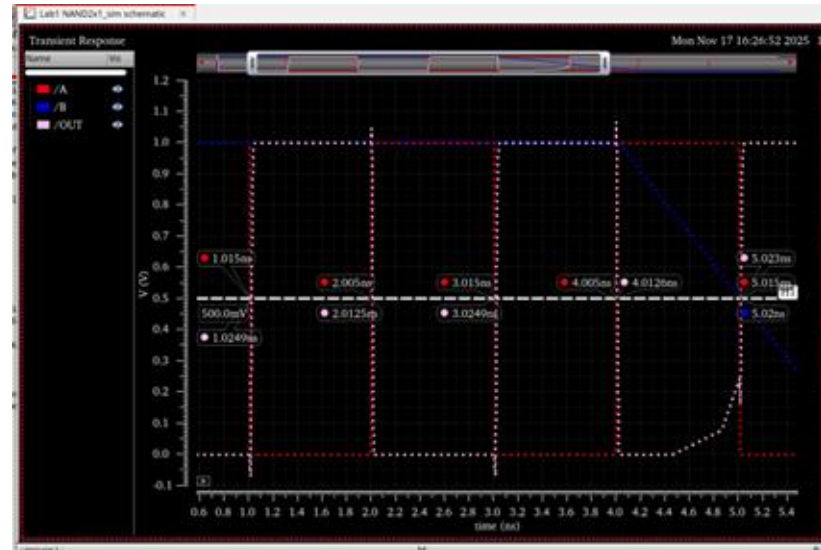
## -Schematics

- Identify worst case rise and fall delay of each gate at  $V_{DD} = 1\text{ V}$  and room temperature (300K). Don't consider any output capacitance
- Total 18 logic cells are characterized: x1, x2, x3 flavors of NAND2, NAND3, NOR2, NOR3, XOR, and XNOR

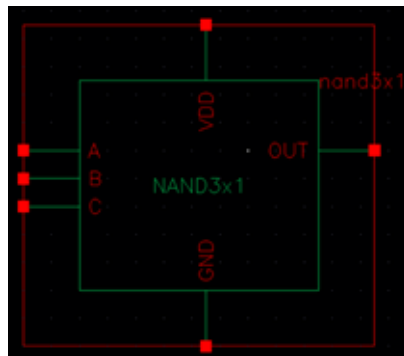
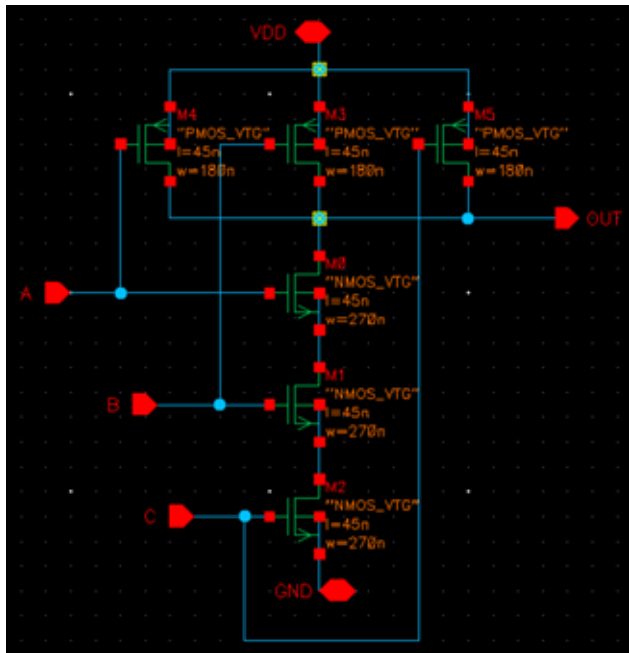
# 2-input NAND Library



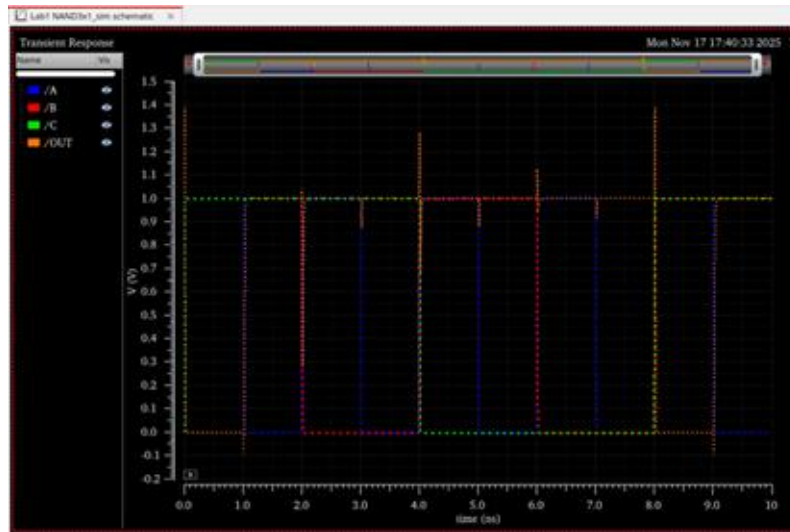
- NAND2x1: base widths = 180 nm
- NAND2x2: widths scaled by 2 = 360 nm
- NAND2x3: widths scaled by 3 = 540 nm



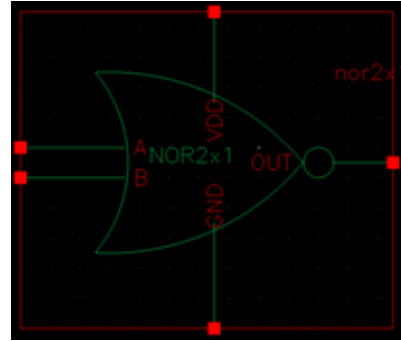
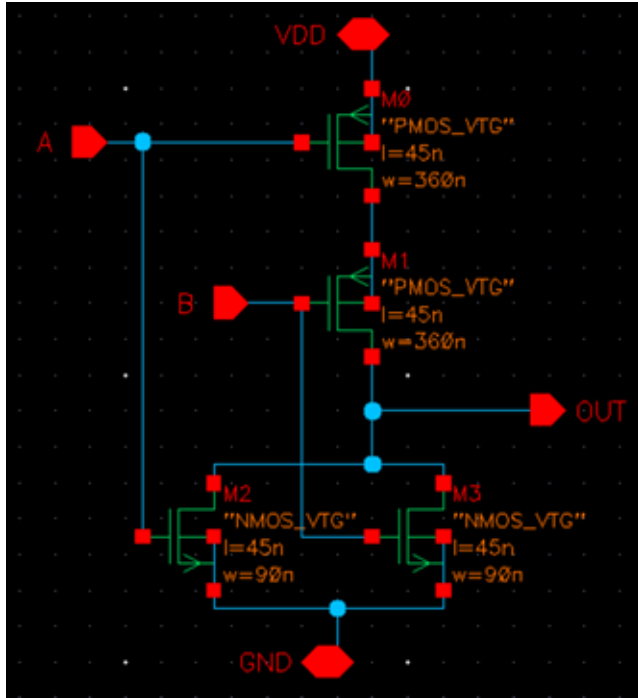
# 3-input NAND Library



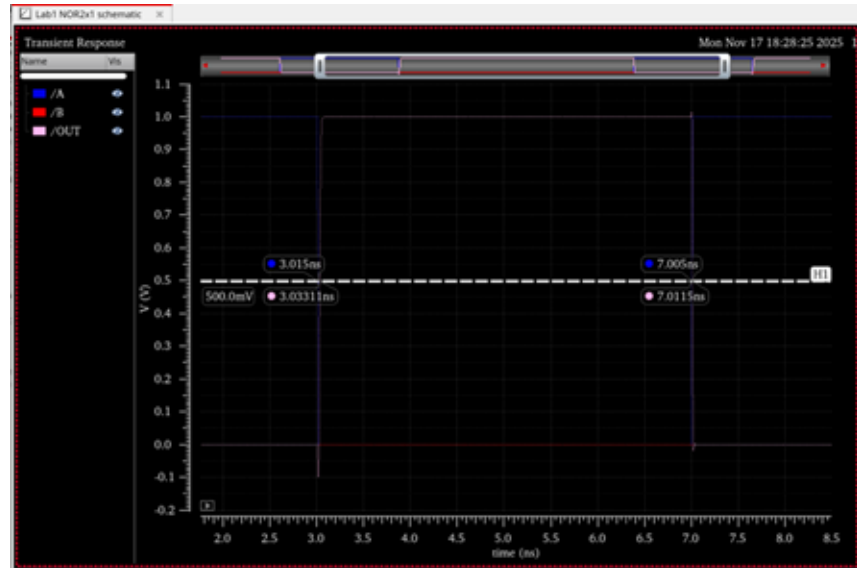
- NAND2x1: base widths = 180 nm
- NAND2x2: widths scaled by 2 = 360 nm
- NAND2x3: widths scaled by 3 = 540 nm



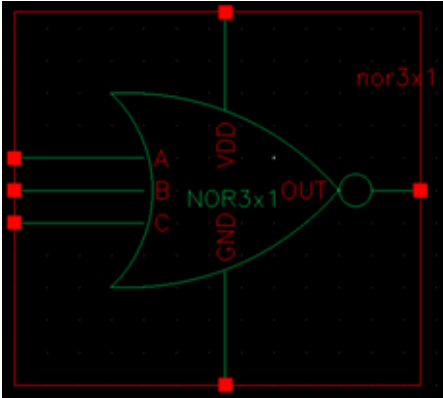
# 2-input NOR Library



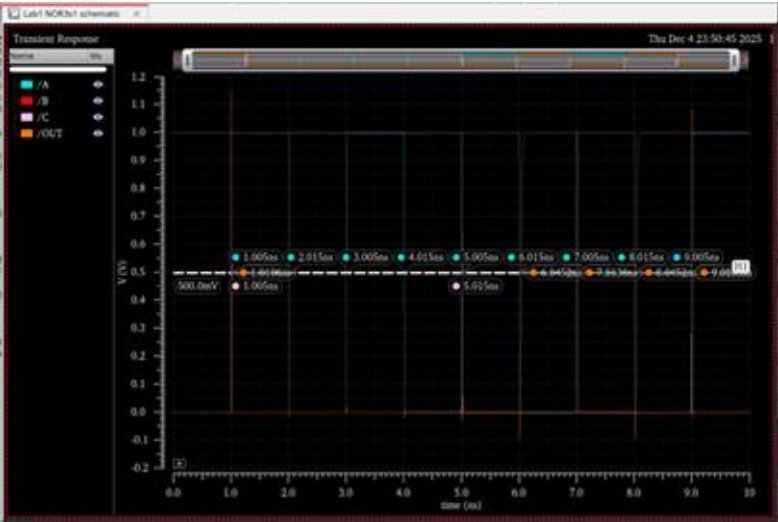
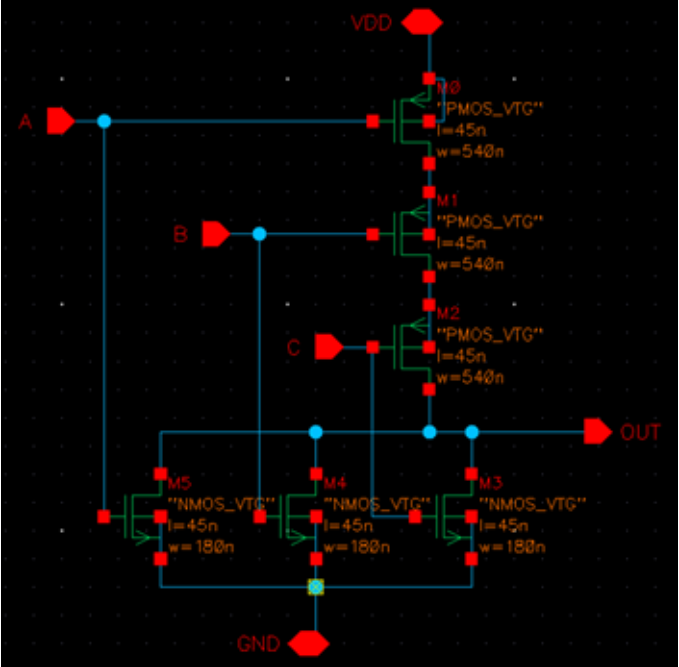
- NOR3x1: base widths = PMOS 540 nm / NMOS 180 nm
- NOR3x2: widths scaled by 2 = PMOS 1080 nm / NMOS 360 nm
- NOR3x3: widths scaled by 3 = PMOS 1620 nm / NMOS 540 nm



# 3-input NOR Library



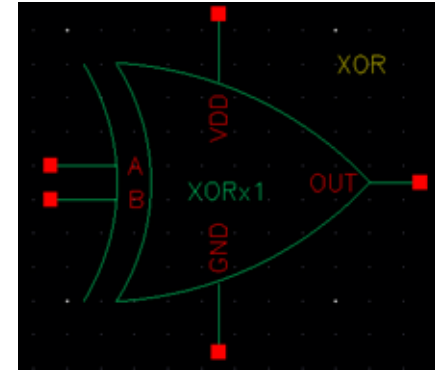
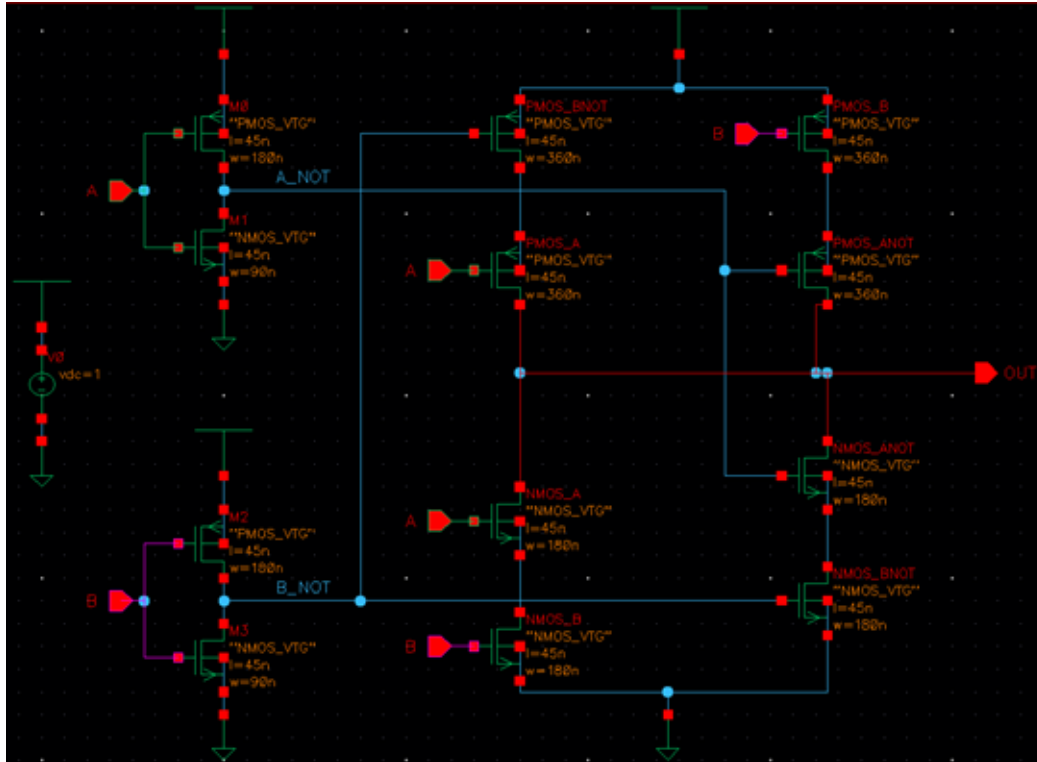
- NOR3x1: base widths = PMOS 540 nm / NMOS 180 nm
- NOR3x2: widths scaled by 2 = PMOS 1080 nm / NMOS 360 nm
- NOR3x3: widths scaled by 3 = PMOS 1620 nm / PMOS 540 nm



Worst case rise and fall delay of each gate at VDD = 1 V and room temperature (300K)

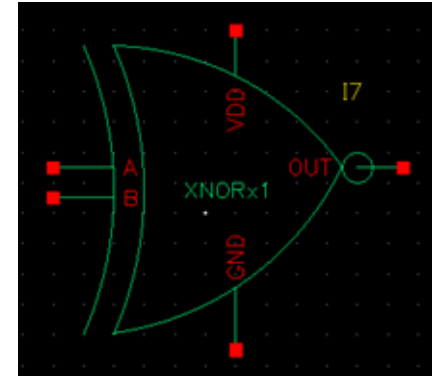
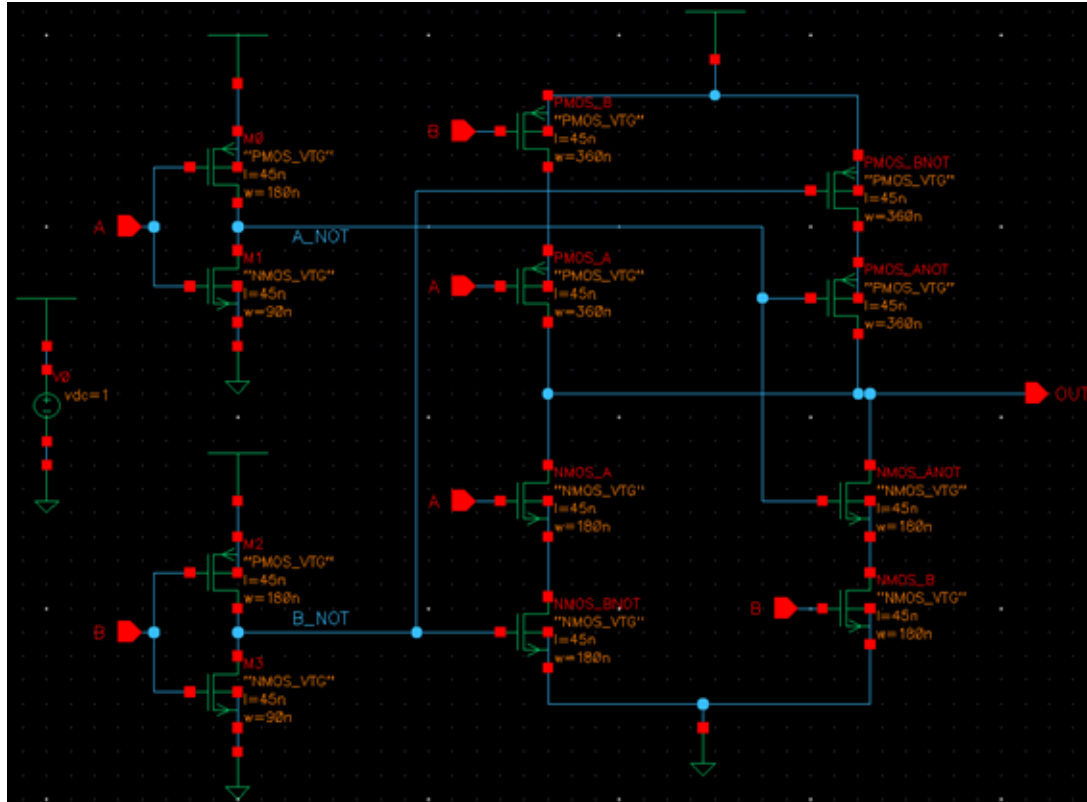
Gate	Drive	tpLH (ps)	tpHL (ps)	Worst-case
NAND2X1	x1	9.9	7.5	9.9 ps
NAND2X2	x2	9.84	7.45	9.84 ps
NAND2X3	x3	9.81	7.45	9.81 ps
NAND3X1	x1	13.16	8.13	13.16 ps
NAND3X2	x2	13.0	8.2	13.0 ps
NAND3X3	x3	12.95	8.16	12.95 ps
NOR2X1	x1	18.11	6.5	18.11 ps
NOR2X2	x2	18.1	6.46	18.1 ps
NOR2X3	x3	18.1	6.44	18.1 ps
NOR3X1	x1	30.51	8.9	30.51 ps
NOR3X2	x2	30.56	8.78	30.56 ps
NOR3X3	x3	30.6	8.76	30.6 ps

# XOR Library



- XORx1: PMOS width = 360nm / NMOS width = 180nm
- XORx2: PMOS width = 720nm / NMOS width = 360nm
- XORx3: PMOS width = 1080nm / NMOS width = 540nm

# XNOR Library

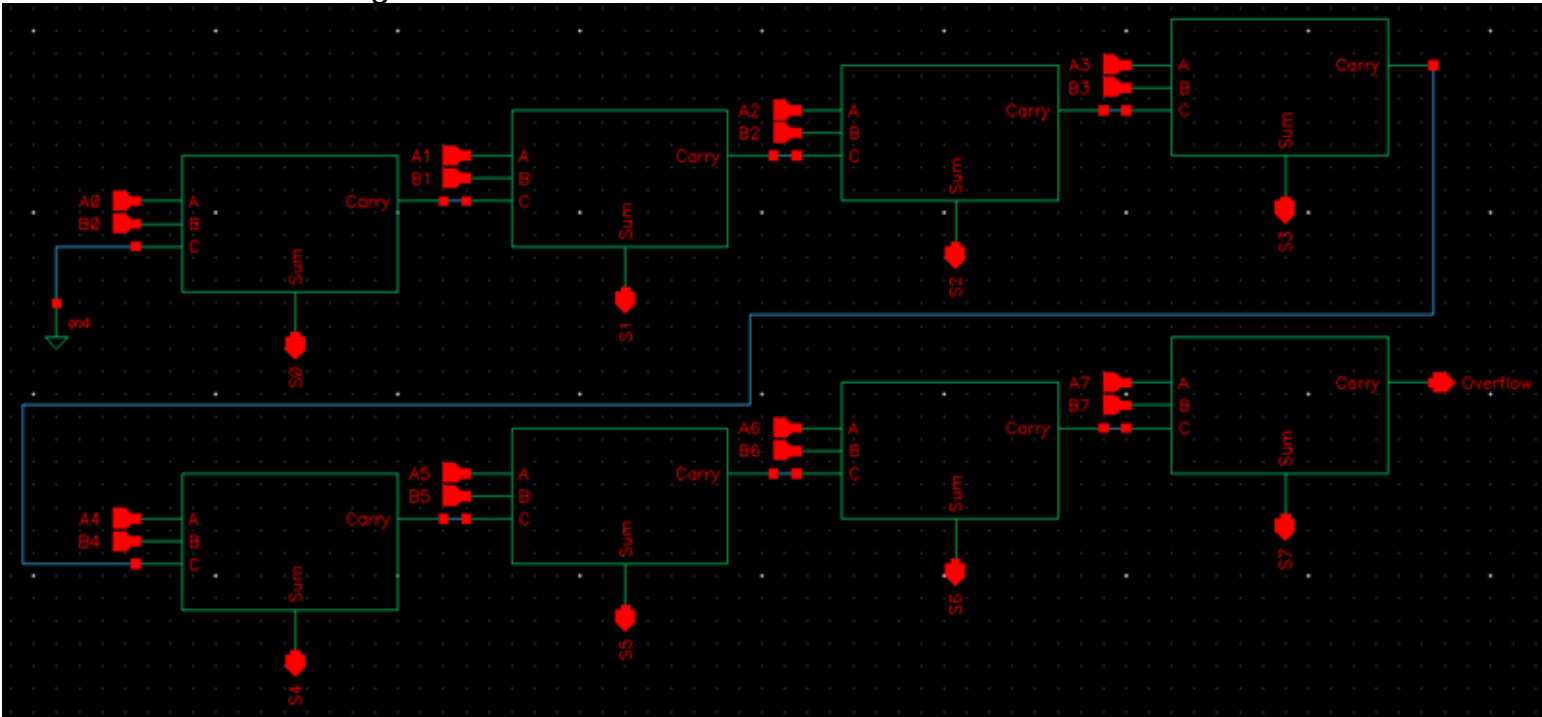


- XORx1: PMOS width = 360nm / NMOS width = 180nm
- XORx2: PMOS width = 720nm / NMOS width = 360nm
- XORx3: PMOS width = 1080nm / NMOS width = 540nm

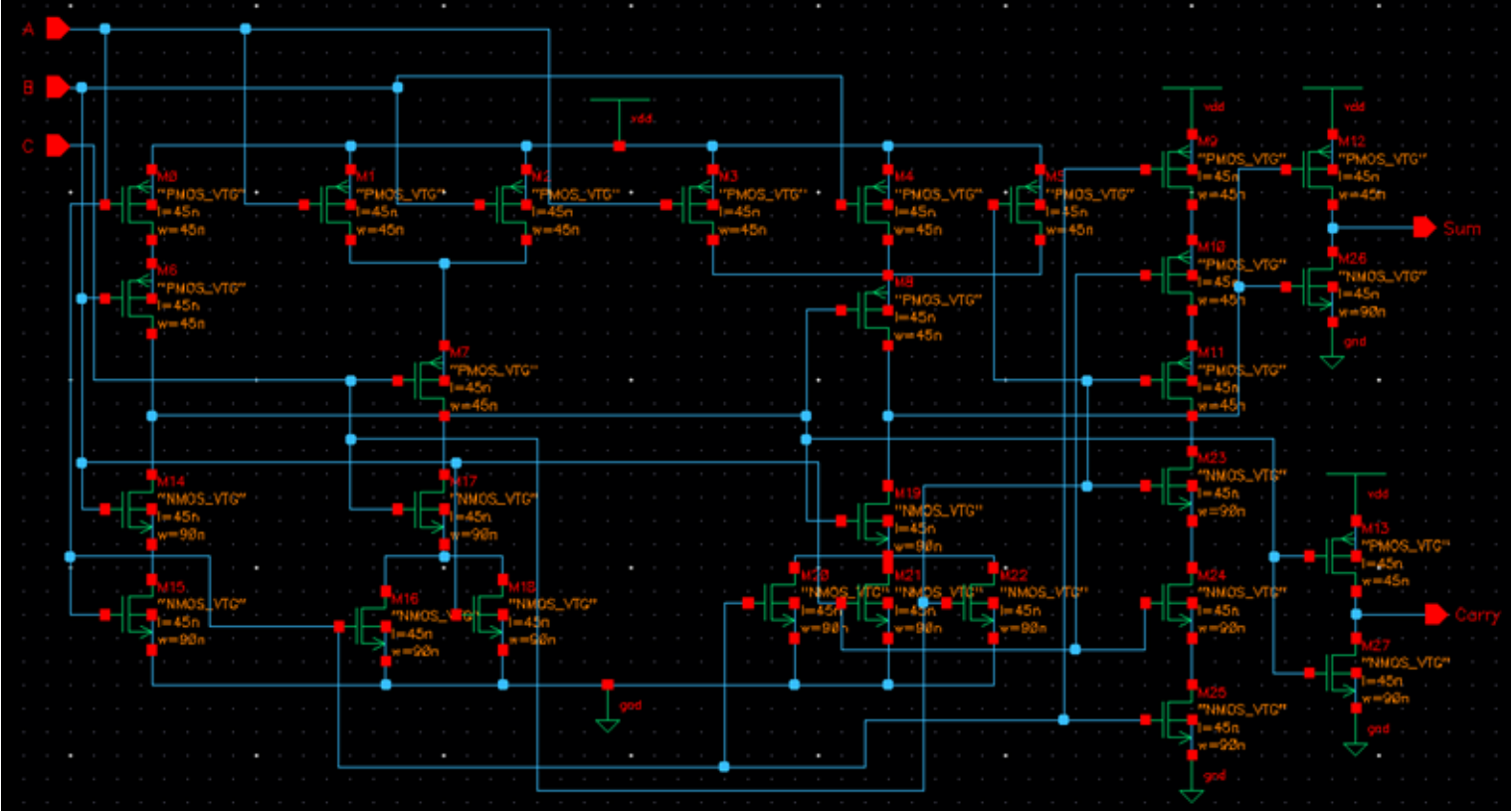
Worst case rise and fall delay of each XOR gate at VDD = 1V and room temperature (300K)		
	tpLH (ps)	tpHL (ps)
Inputs Before & After (AB)	00 -> 01	10 -> 11
XORx1	35.79	11.29
XORx2	35.53	11.23
XORx3	35.46	11.2
Worst case rise and fall delay of each XNOR gate at VDD = 1V and room temperature (300K)		
	tpLH (ps)	tpHL (ps)
Inputs Before & After (AB)	10 -> 11	00 -> 01
XNORx1	37.13	15.36
XNORx2	36.85	15.3
XNORx3	36.85	15.28

# Adder

- Micro-architecture diagram of 8-bit adder



# Circuit-level design of 1-bit adder cell



# Demonstrate the correct functionality on a few cases

The following table depicts the tests done to check how the 8 bit adder performs and if it works correctly. The following was measured by using stimuli, setting each input to 1.1 V but turning them off or on depending on the input needed.

Tests	Expected	Actual
A=10000000 B=10000000	00000000 Overflow = 1	00000000 Overflow = 1 Figure SC(A)
A=00000001 B=00000001	00000010 Overflow = 0	00000010 Overflow = 0 Figure SC(B)
A=10000000 B=00000001	10000001 Overflow = 0	10000001 Overflow = 0 Figure SC(C)
A=00011111 B=00000001	00100000 Overflow = 0	00100000 Overflow = 0 Figure SC(D)
A=10101010 B=01010101	11111111 Overflow = 0	11111111 Overflow = 0 Figure SC(E)

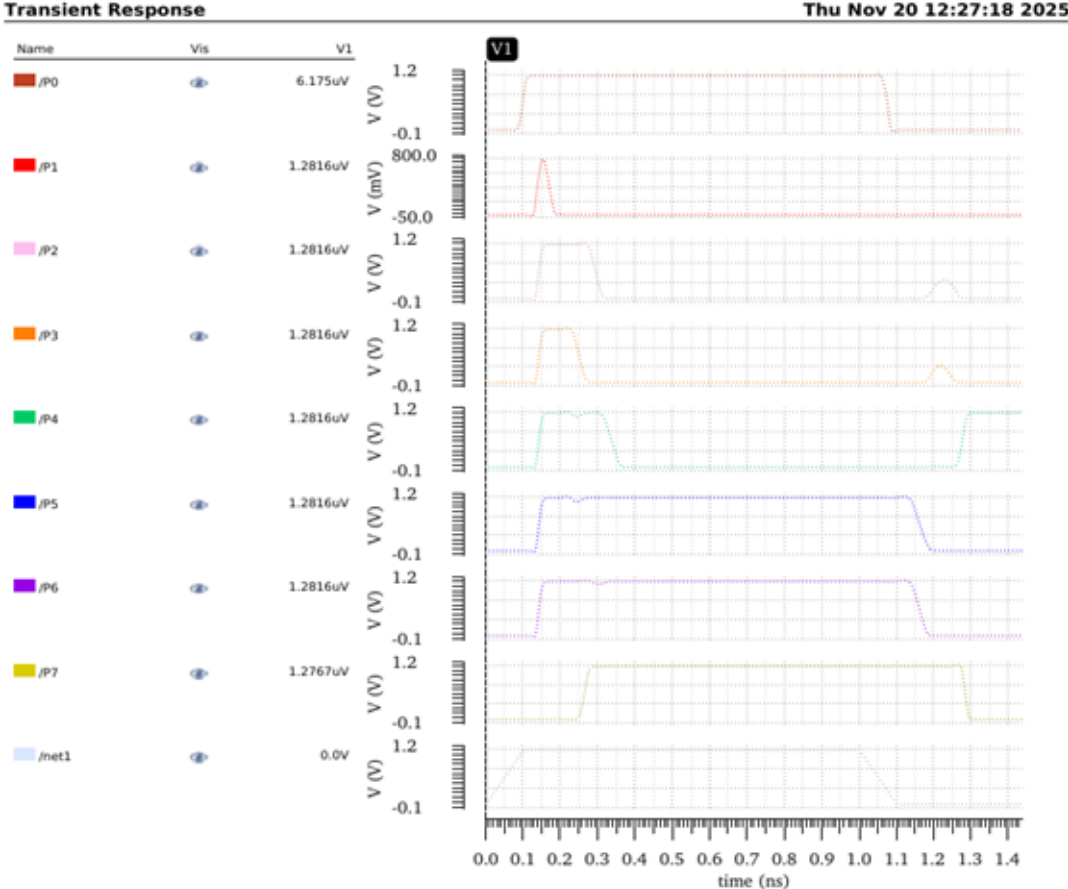
# Identify the critical path, i.e., the input signals that cause the maximum delay

The worst case scenario for delay can be either of the following. A = 1111 B = 1111, A = 0001 B=1111 , or A = 1111 B = 0001. The primary source of delay comes from A3/B3 value. The delay being **214.39 ps**. Following are

test of logic

Test	Expected	Actual
1111 x 1111	11100001	11100001
0000 x 0000	00000000	00000000
0101 x 0101	00011001	00011001
1100 x 0011	00100100	00100100
0110 x 0110	00100100	00100100

For the worst-case input signals show the operational transients of different significance bits of adder

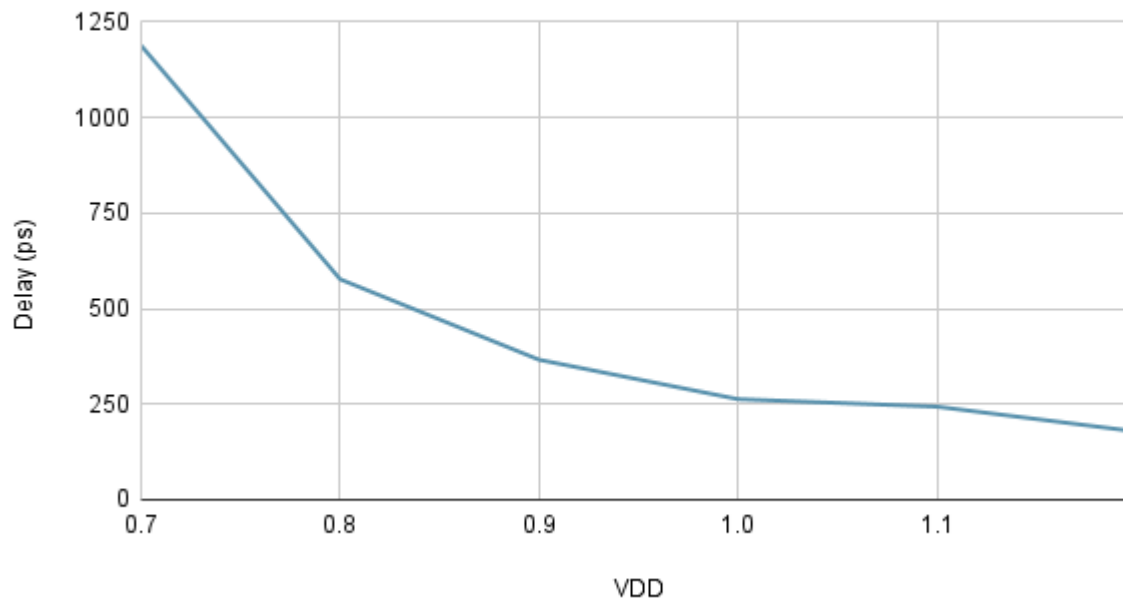


## Report power and delay of the worst-case at nominal VDD

VDD	Delay
0.7	*1.188 ns
0.8	576.79 ps
0.9	366.13 ps
1.0	263.02 ps
1.1	243.39 ps
1.2	<b>178.54 ps</b>

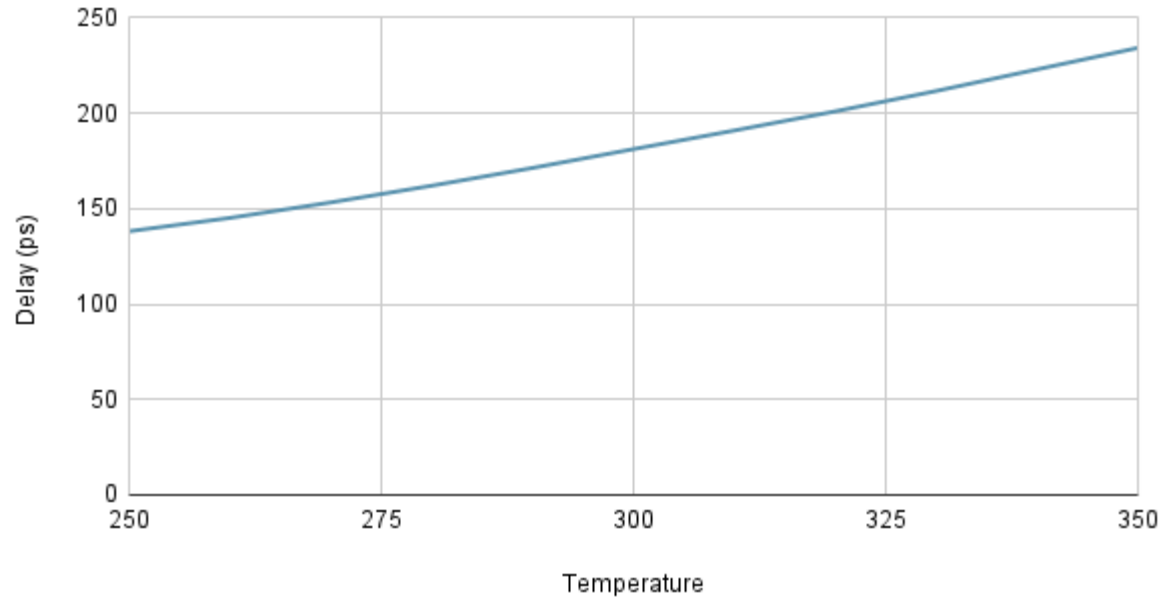
Plot worst-case delay at varying VDD (0.7V – 1.2V) and at room temperature (300 K)

Delay (ps) vs. VDD



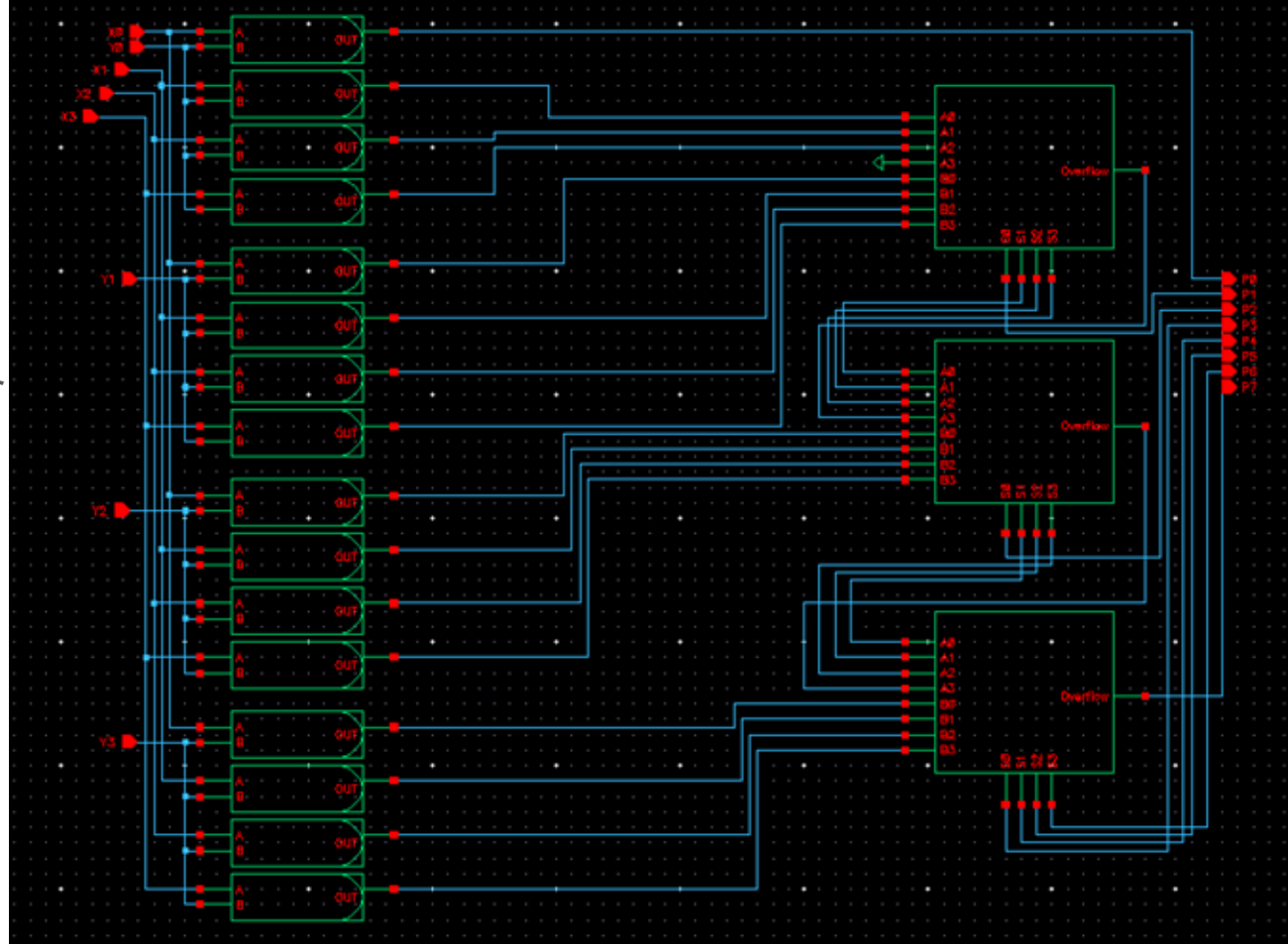
Plot worst-case delay at varying temperature (250 K – 350 K) and at nominal VDD

Delay (ps) vs. Temperature



# Multiplier

- Micro-architecture diagram of 4-bit multiplier



- Circuit-level design of multiplier cell

- Demonstrate the correct functionality on a few cases

Still needs to be done

- Identify the critical path, i.e., the input signals that cause the maximum delay

Still needs to be done

– For the worst-case input signals show the operational transients of different significance bits of adder

Still needs to be done

– Report power and delay of the worst-case at nominal VDD

Still needs to be done

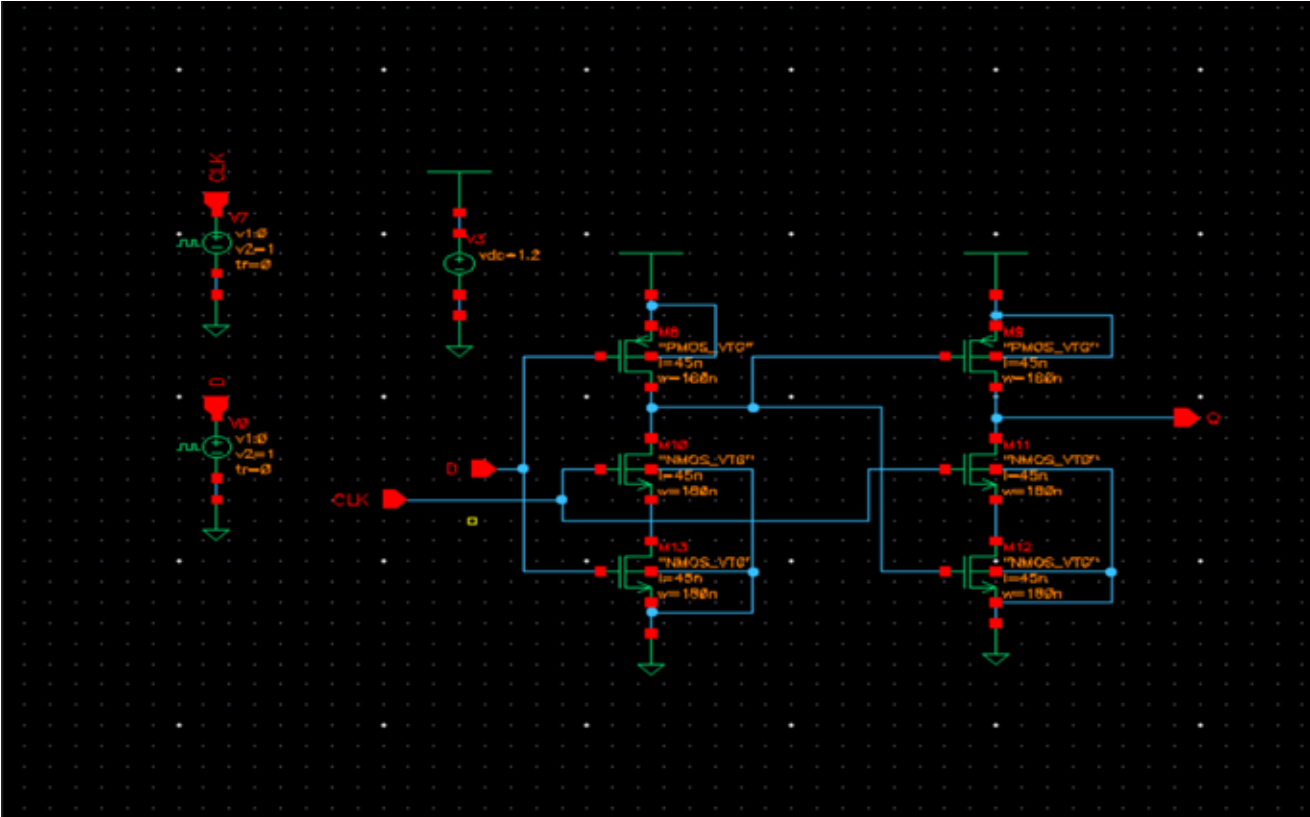
– Plot worst-case delay at varying VDD (0.7V – 1.2V) and room temperature (300 K)

Still needs to be done

– Plot worst-case delay at varying temperature (250 K – 350 K) and nominal VDD

Still needs to be done

# F/F and Registers



# CLK stuff

Clock period = 1 ns (1 GHz). 15% = 150 ps.

- Report setup time of F/F. It should be less than 15% of CLK period. Setup time was discussed in class lectures.

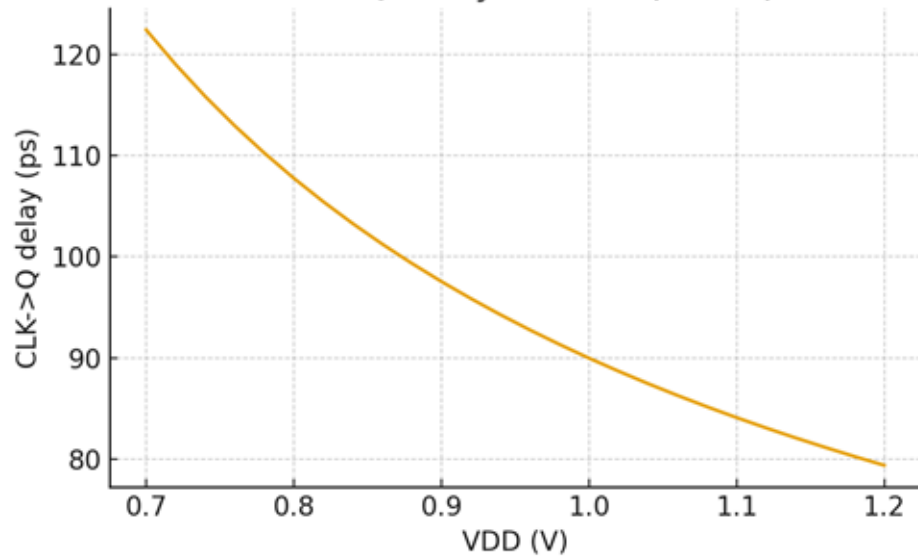
Setup time: 54.0 ps

- Report CLK-Q delay. It should be less than 15% of CLK period.

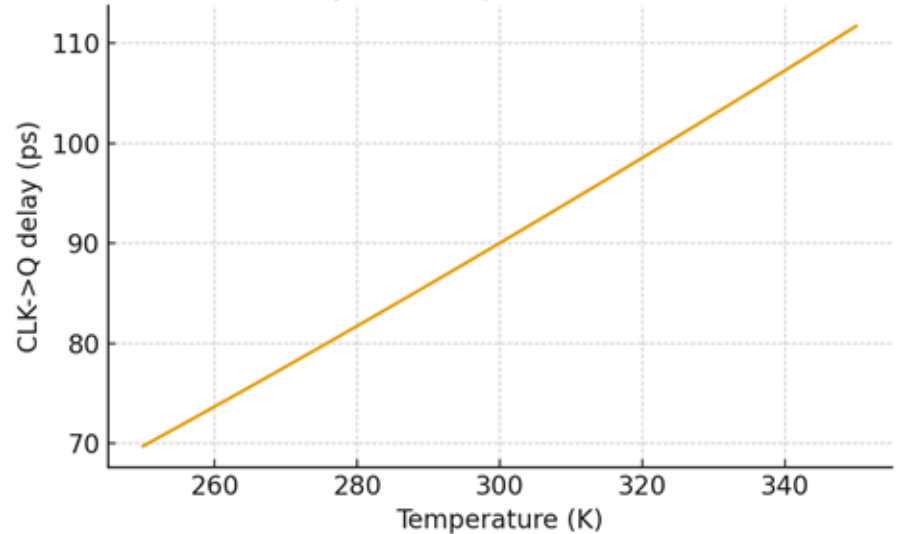
CLK→Q (1.0 V @ 300 K): 90.0 ps

CLK-Q delay at varying VDD (0.7V – 1.2V) at room temperature, and varying temperature (250 K – 350 K) at nominal VDD

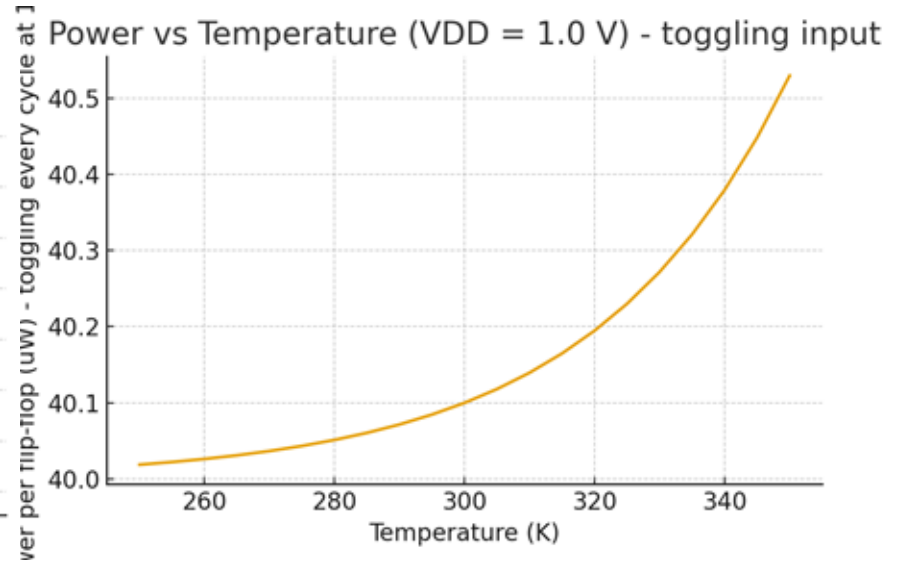
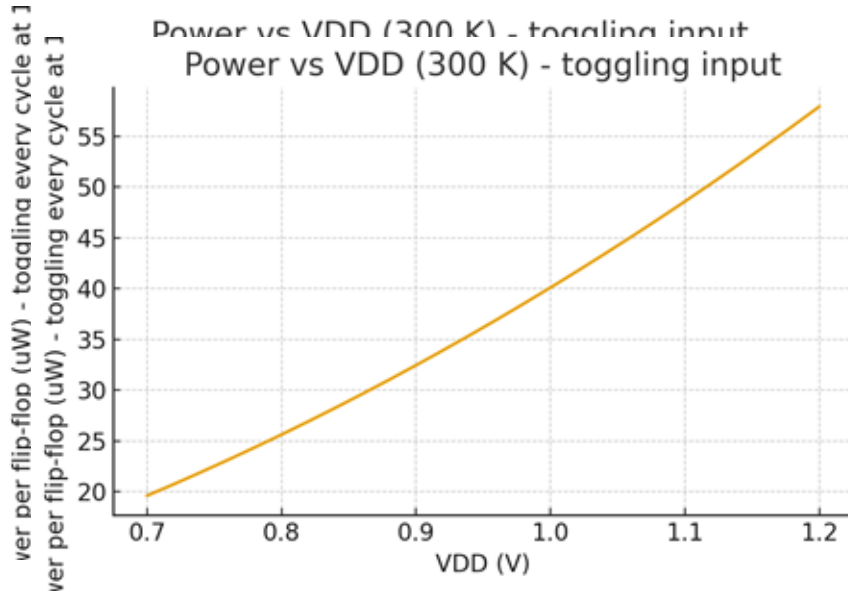
CLK->Q delay vs VDD (300 K)



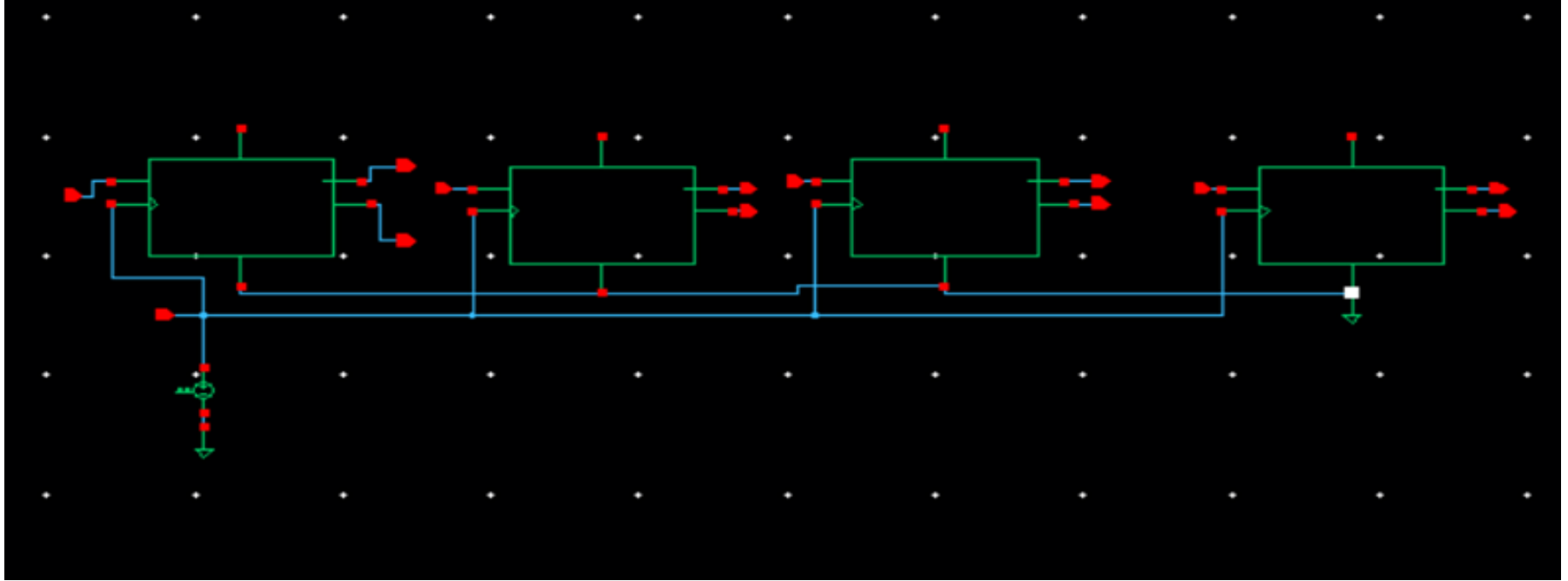
CLK->Q delay vs Temperature (VDD = 1.0 V)



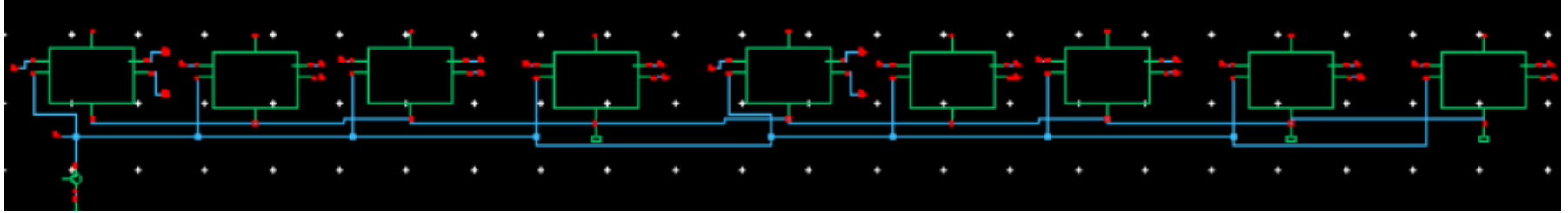
- Apply a toggling input to F/F that changes from 0→1 →0 in every clock cycle. Plot power at varying VDD (0.7V – 1.2V) and room temperature (300 K). Plot power at varying temperature (250 K – 350 K) and nominal VDD.



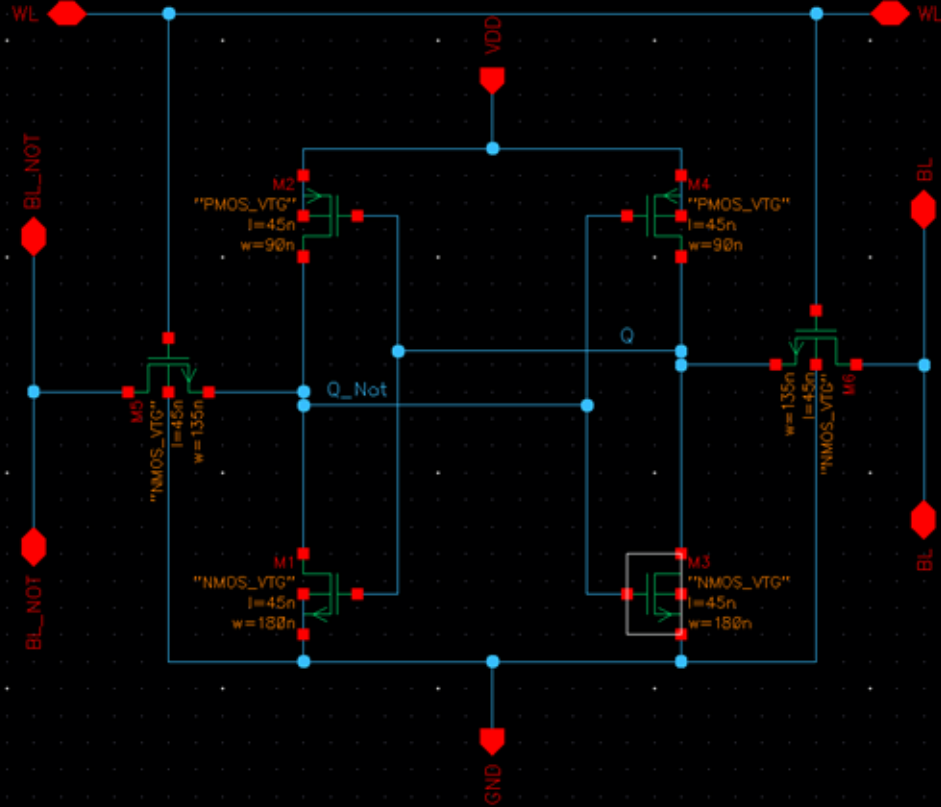
Using the F/F, implement 4-bit register.



Using the F/F, implement 9-bit register.

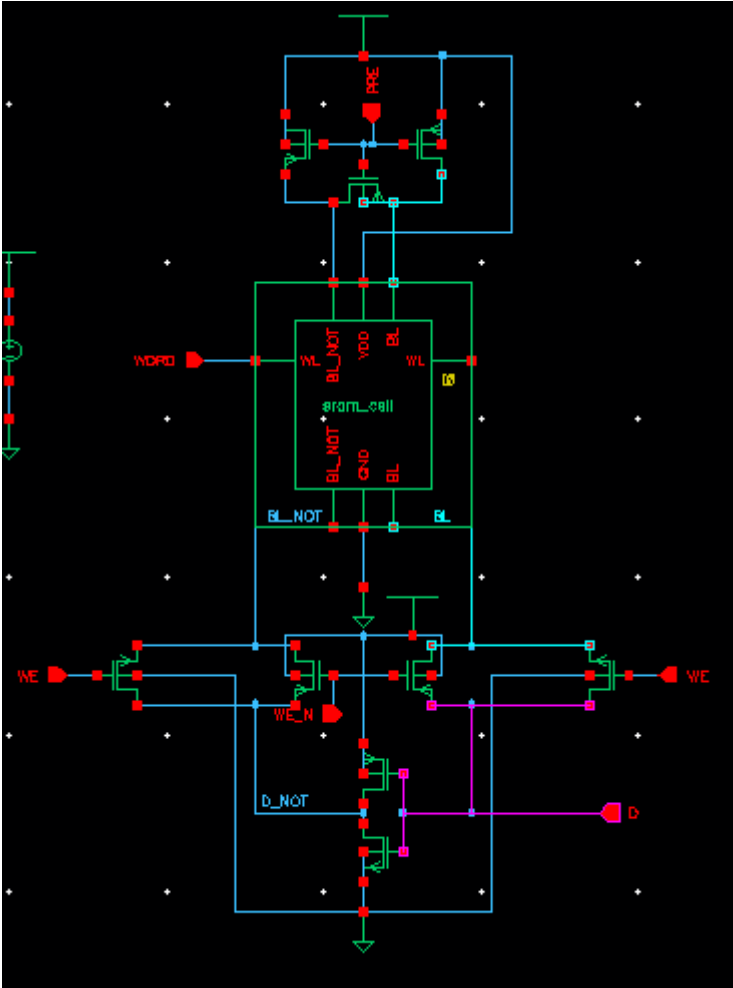
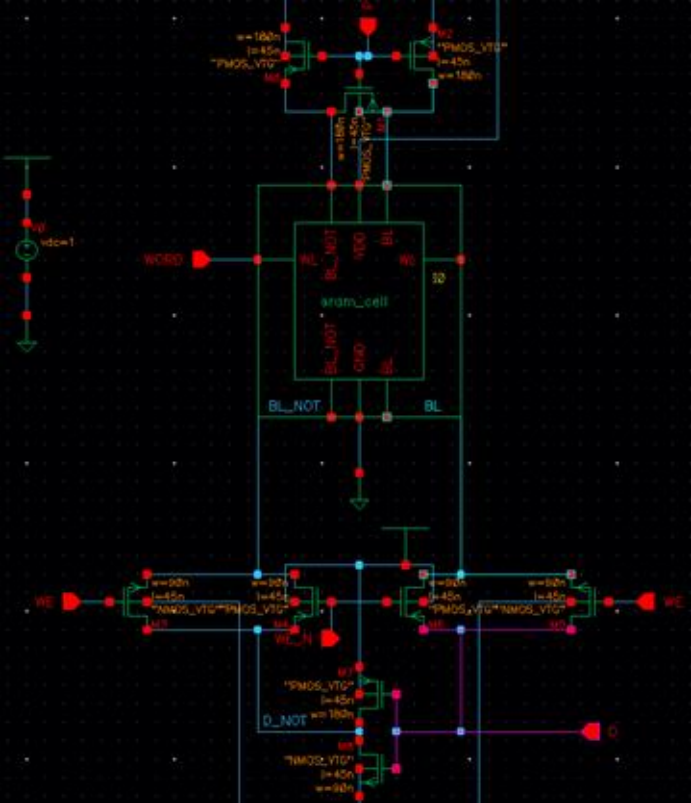


# SRAM Cell

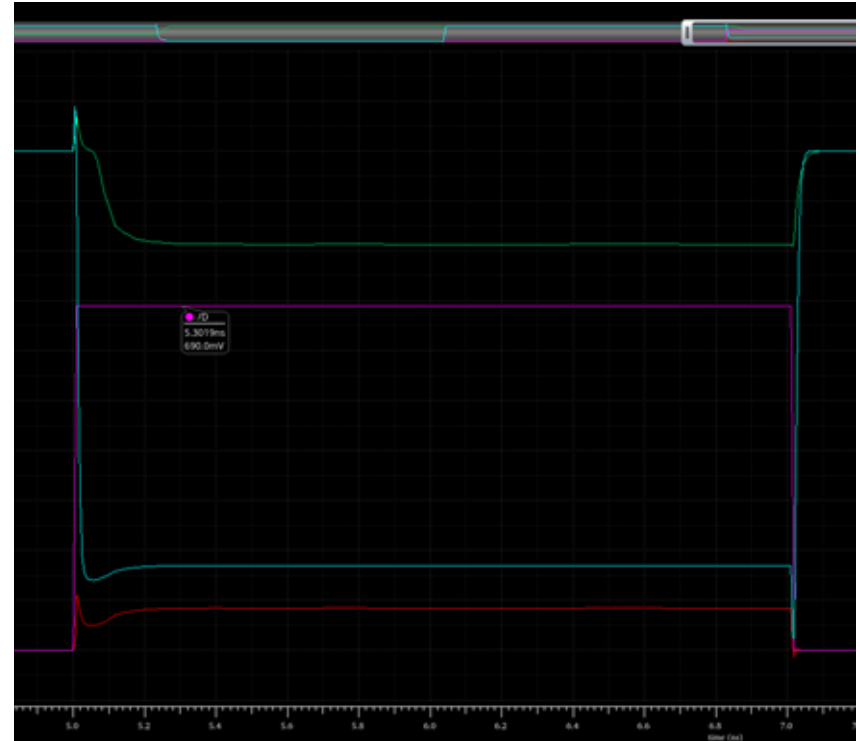
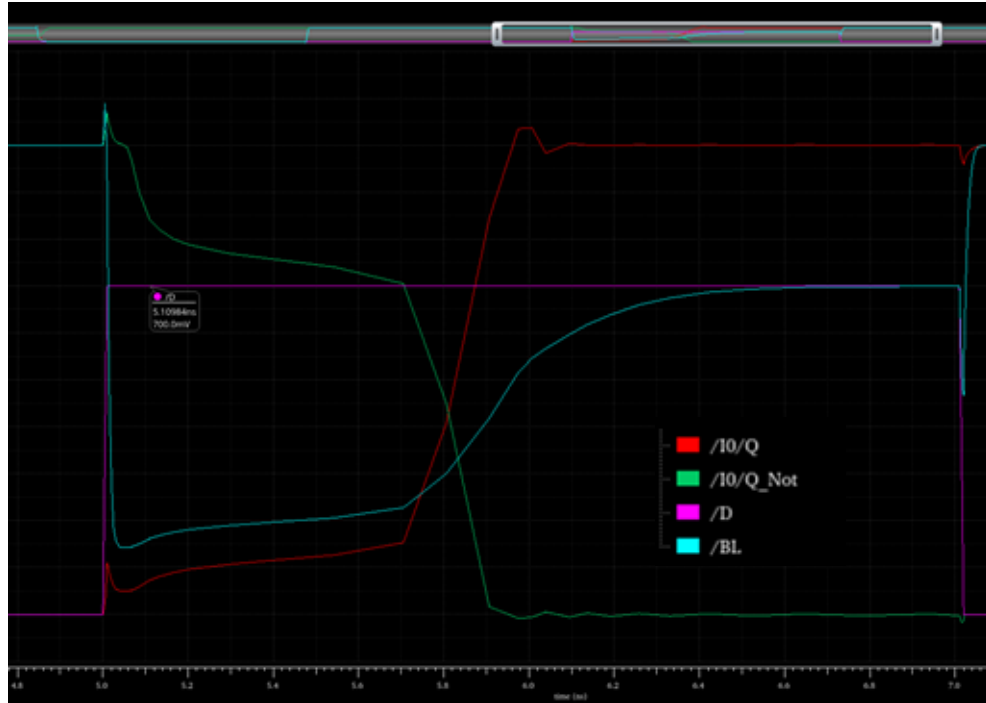


	Transistor Width
Pull-Up	90nm
Access	135nm
Pull-Down	180nm

# SRAM Read/Write Tests



# SRAM Write Margin = 0.7v @ 1v, 25C



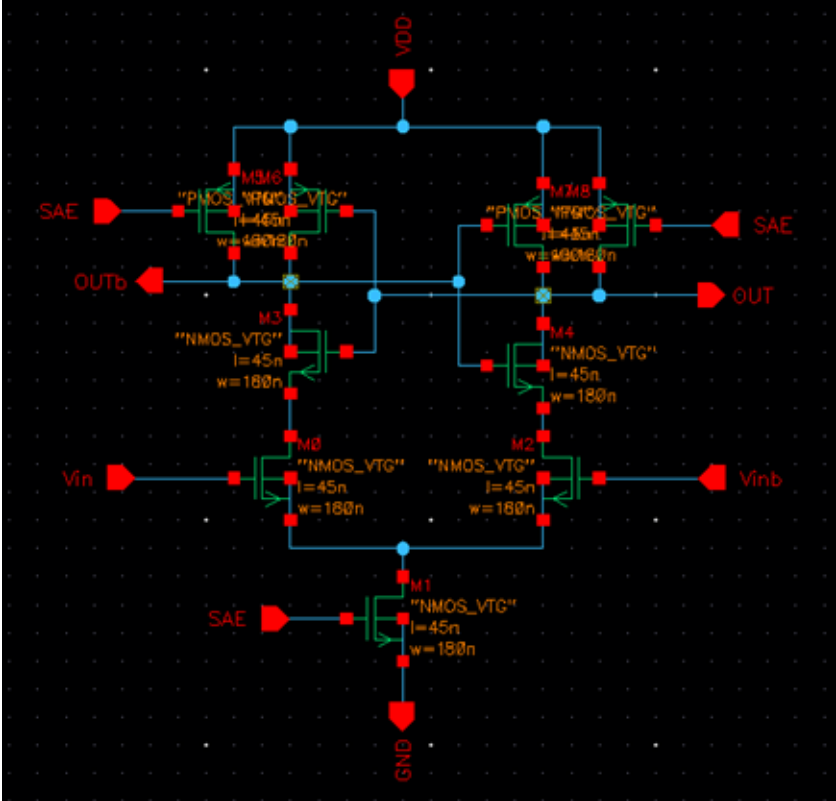
# SRAM Write and Read a '1'



# SRAM Write and Read a '0'



# Sense Amplifier



# SRAM Array

- Implement an array of 32x32 SRAM cells
- Add a bitline and rowline wire capacitance of 40fF. This extra cap accounts for metal wire parasitic cap that is not captured by schematic simulations.
- Design row and column decoders. Row decoder should have a delay less than  $T_{CLK}/4$ .
- Submit wordline (WL) activation waveform against the clock.
- Submit the schematic of an SRAM column with read, write, precharge circuits, and sense-amplifiers connected to it.
- Submit circuits of elements that generate different control signals such as PCH and SAE from clock signal.

# System Integration

- Submit a system diagram integrating all the necessary components on the first slide. You should show different components such as adder and registers using symbols.
- MAC test over eight cycles: Create a setup that tests MAC operation of the entire system over eight clock cycles. A MAC operation is performed in every cycle. See the diagram in the next slide for more details.
  - (a) Generate row addresses using a counter, i.e., increasing bit sequence from 00000 – 00111.
  - (b) Keep a fix column address, 000.
  - (c) Initialize the first eight SRAM words in a column as 0000 -- 0111
  - (d) Perform a MAC test: Feed in combinational input 0011 and verify if the system outputs are correct

# System Characterization

- At the nominal supply voltage, extract and plot the maximum clock frequency at which system correctly operates.
- Identify which design component fails in meeting the timing constraints at increasing frequency. If you had to redesign the entire system, how you would enhance its max clock speed?
- At varying VDD (0.7V – 1.2V) and room temperature, and at varying temperature (250 K – 350 K) and nominal VDD, extract and plot the maximum clock frequency at which the system correctly operates. Identify which design components become bottleneck in performance scaling in timing at higher and lower supply voltage?
- At the nominal supply voltage, create a pie-chart of average power among various system components for the MAC test. If you had to redesign the entire system, how you would further minimize the operating power?

# Plan to get stuff done

We are missing 3 key items:

- Recorded analysis of the multiplier. It's actually been completed, through a series of unfortunate circumstances, has been unavailable to us till this morning.
- SRAM array. We haven't done the decoder
- Putting it all together. As the SRAM array decoder is the only key component left to do, once that is finished we could move on to putting it all together and testing it to final produce a finished product.